

Figure 1

F05080 : 66272660

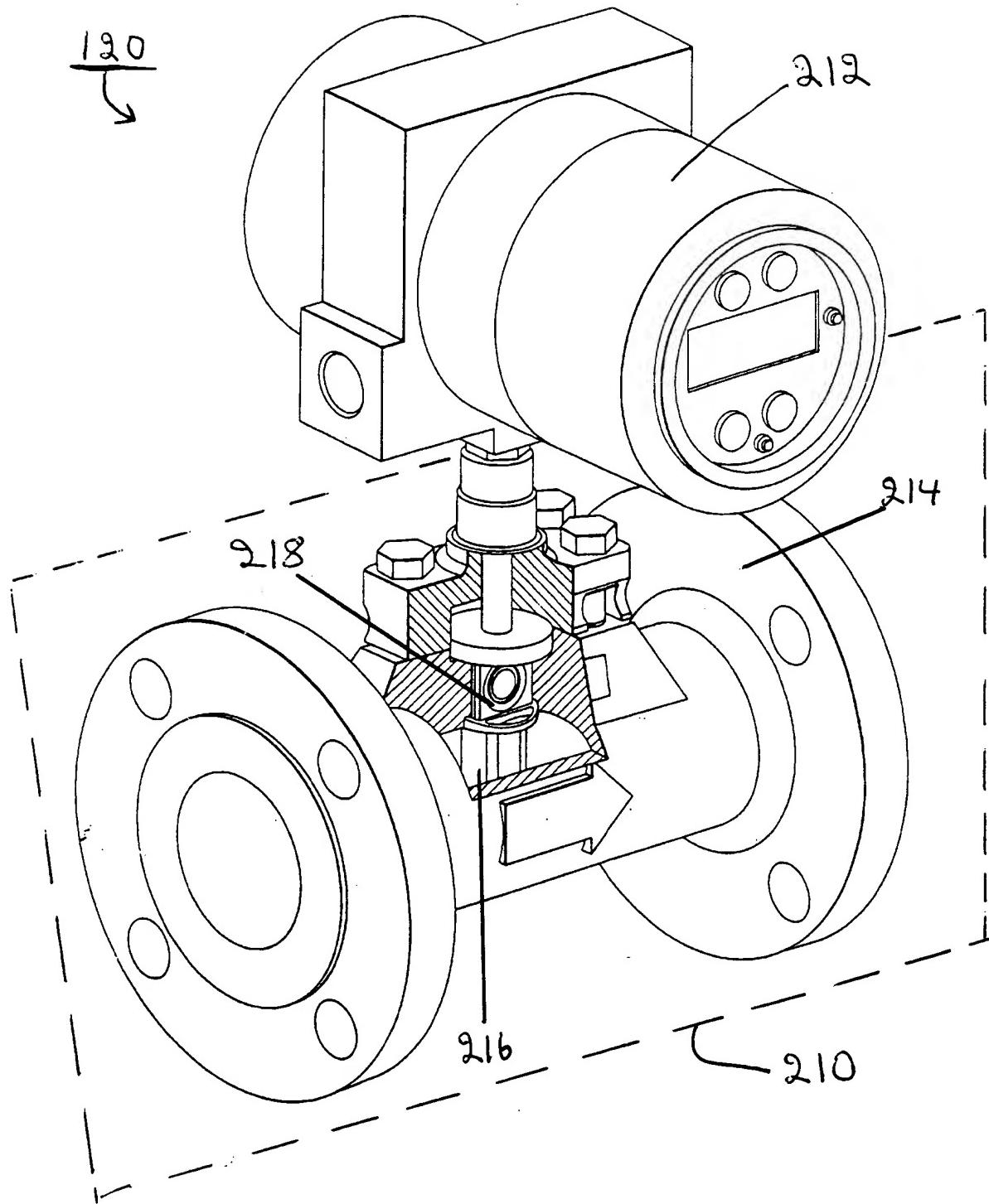


Figure 2

000000000000000000000000

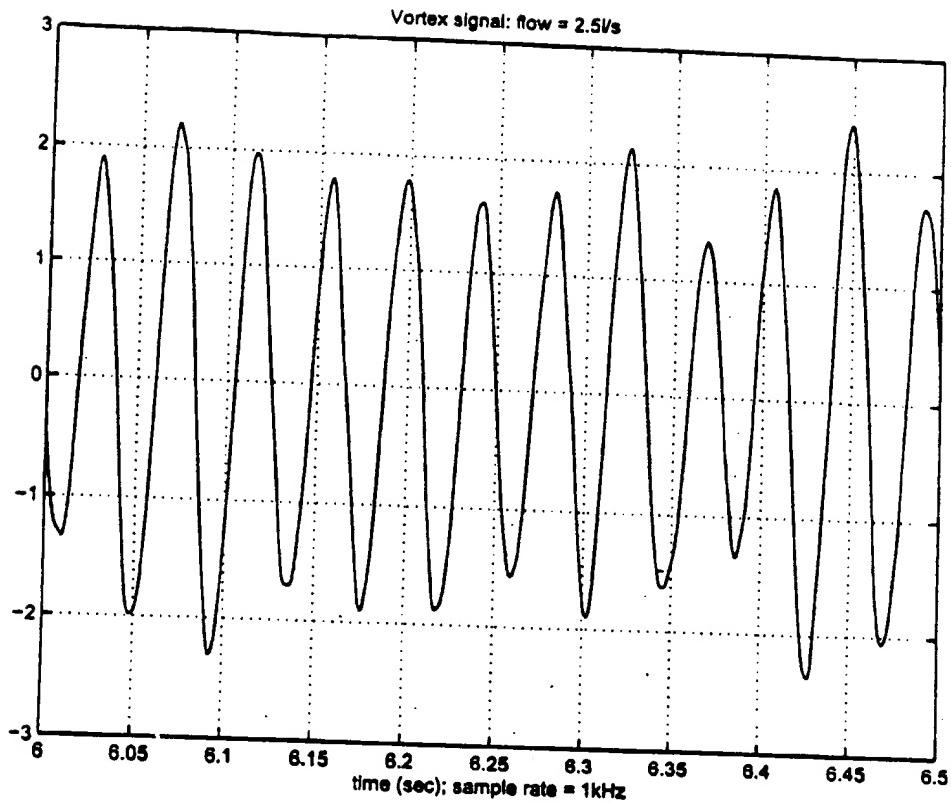


Figure 3a

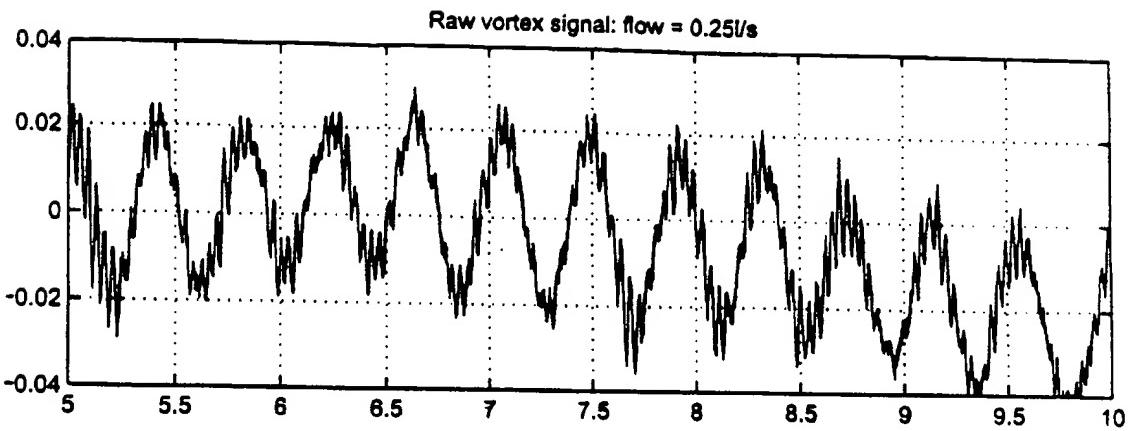


Figure 3 b

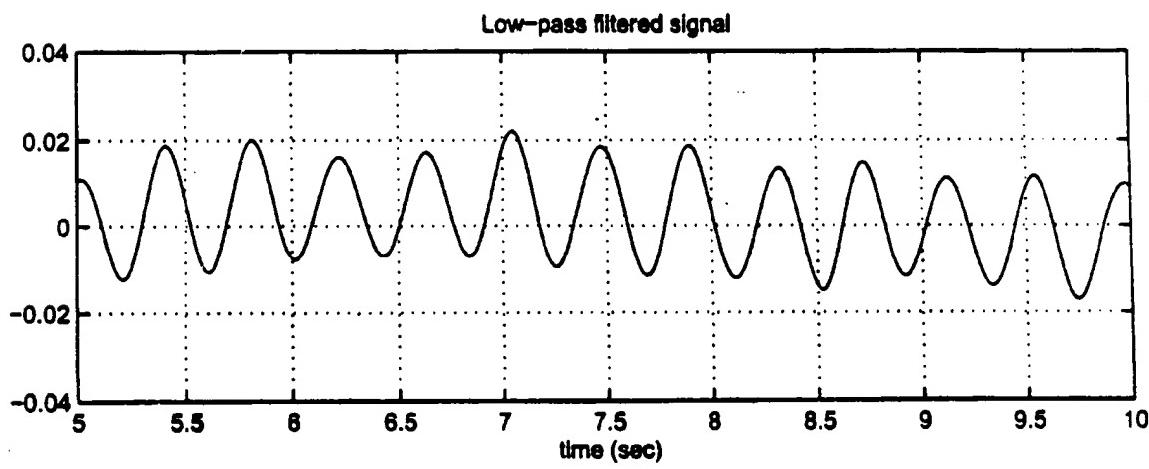
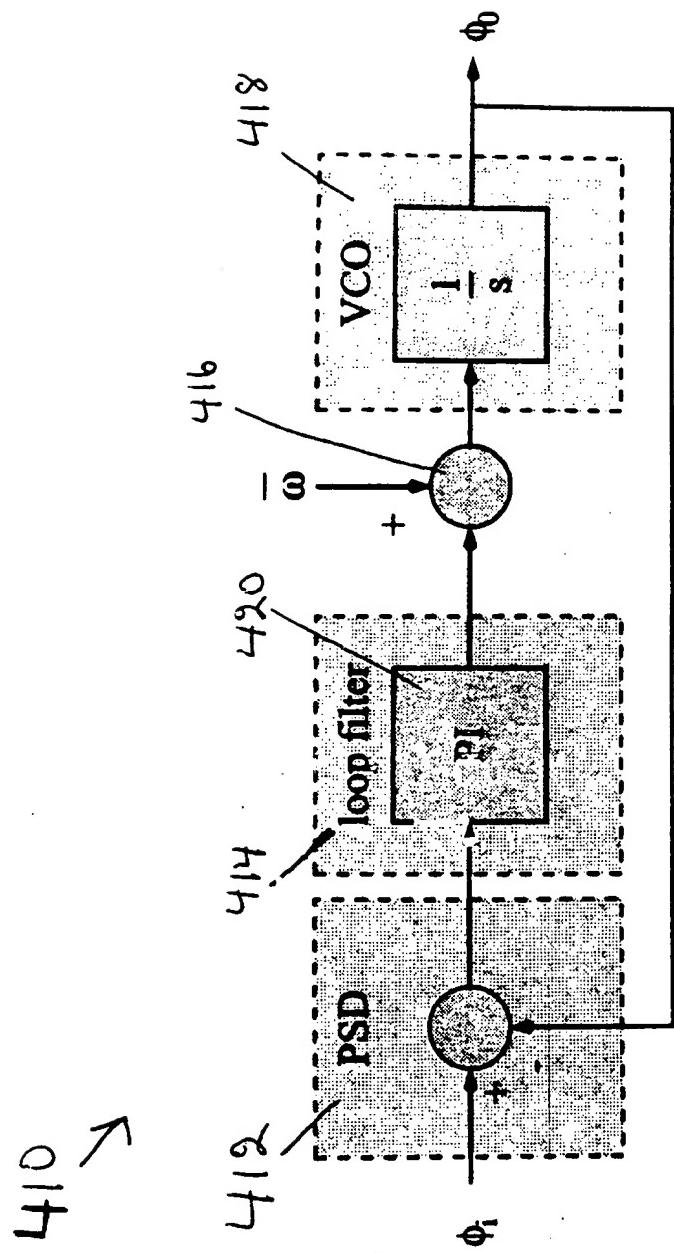


Figure 3 c

Figure 4



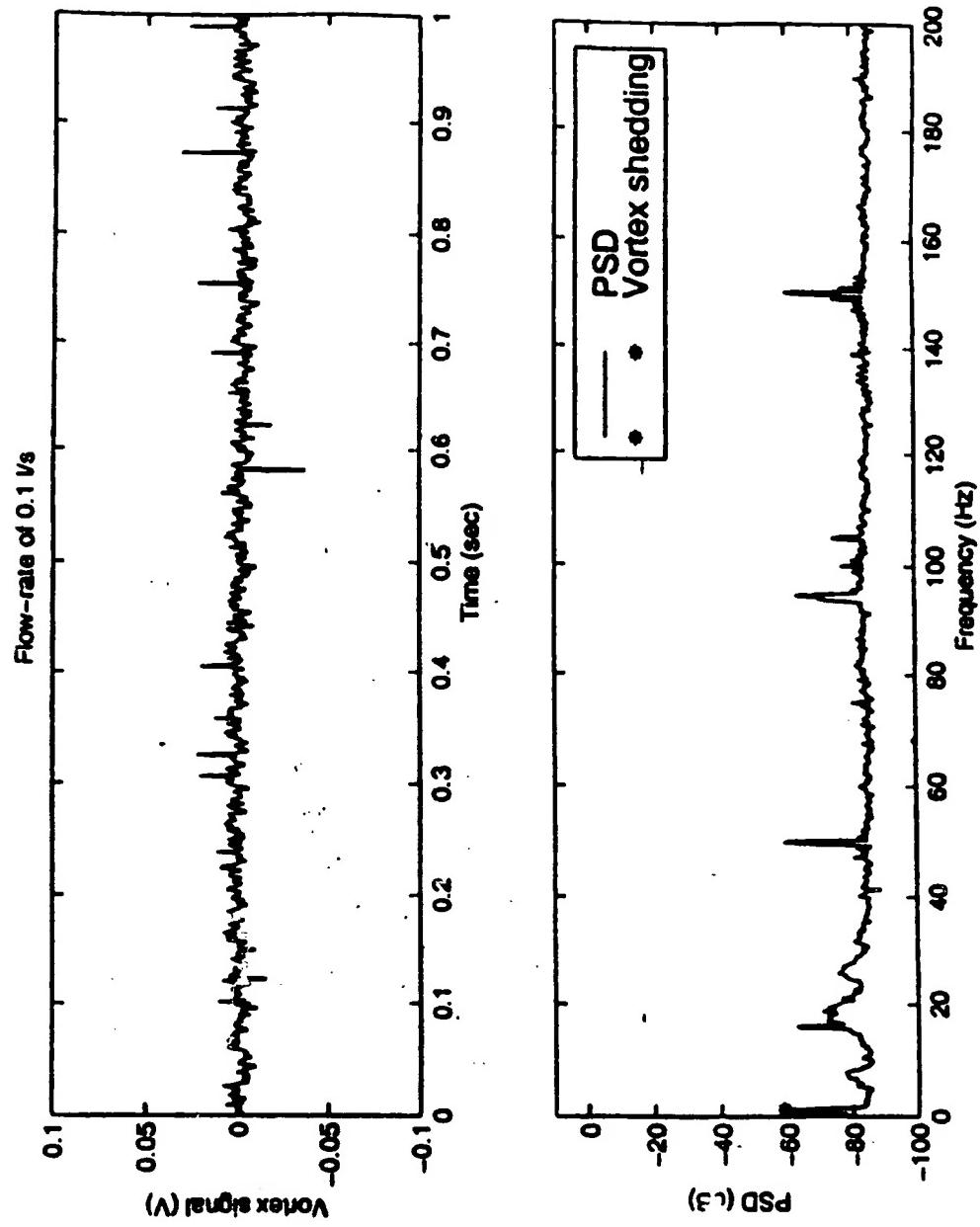
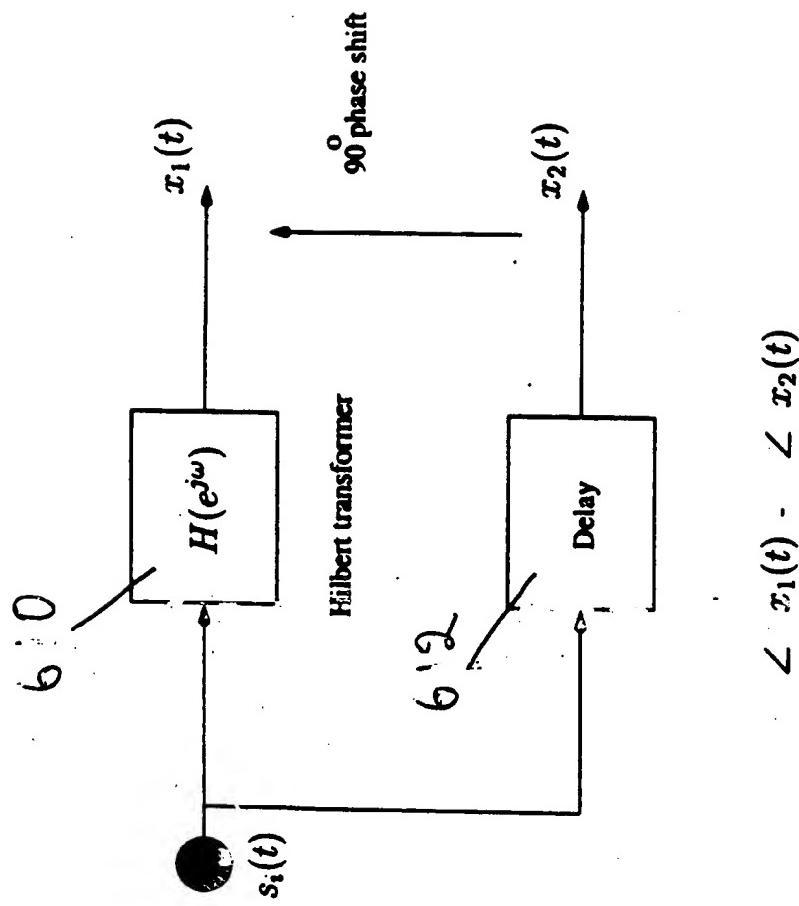


Figure 5



$$\angle x_1(t) - \angle x_2(t)$$

Figure 6

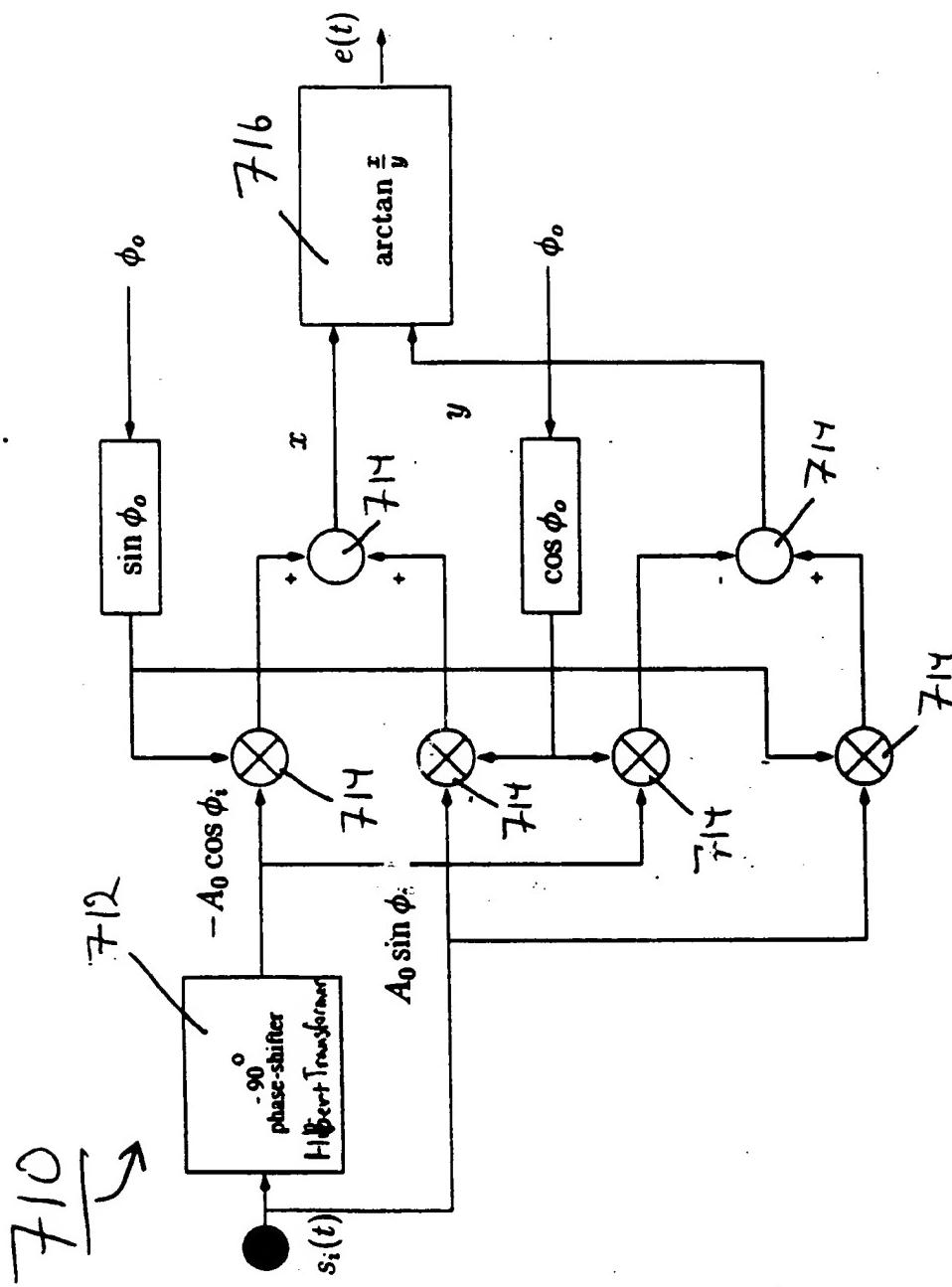


Figure 7

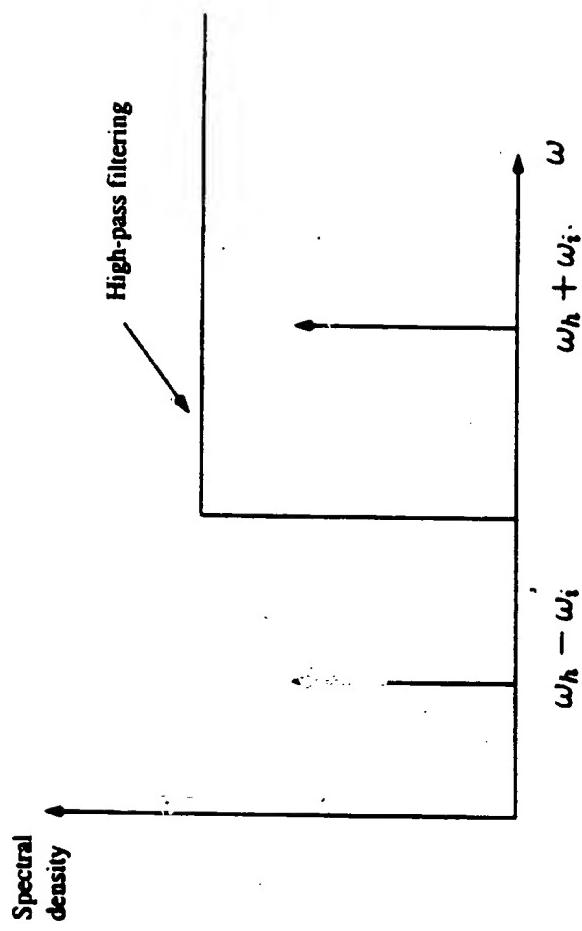


Figure 8

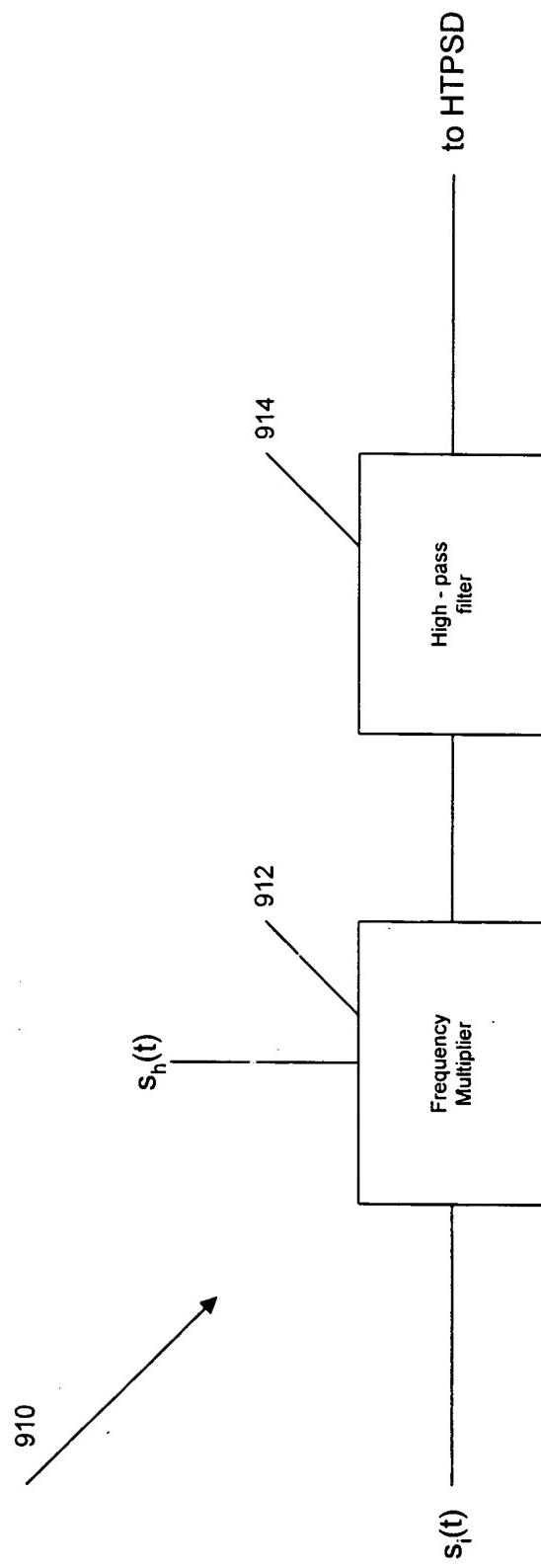


Figure 9

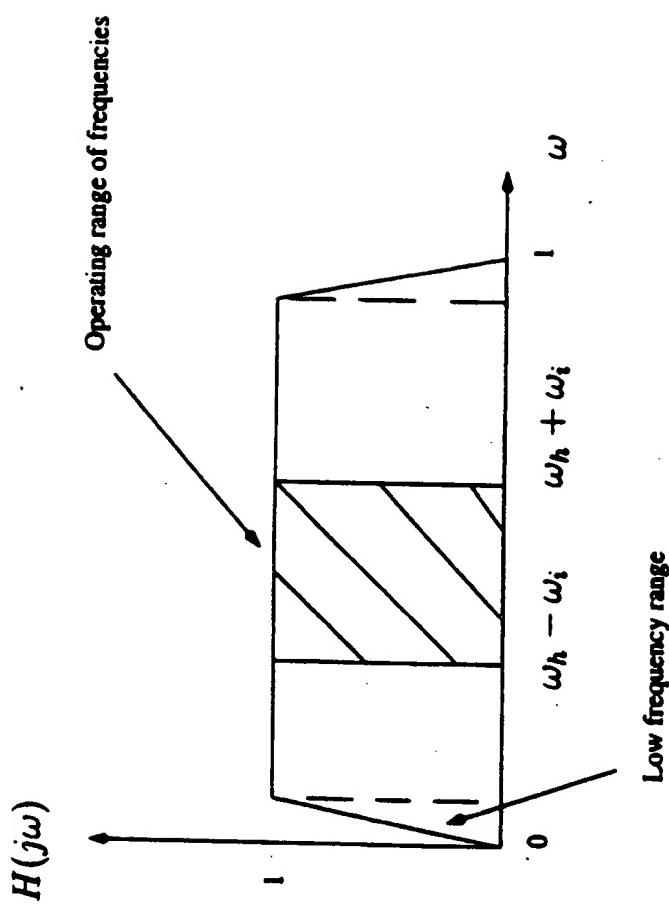


Figure 10

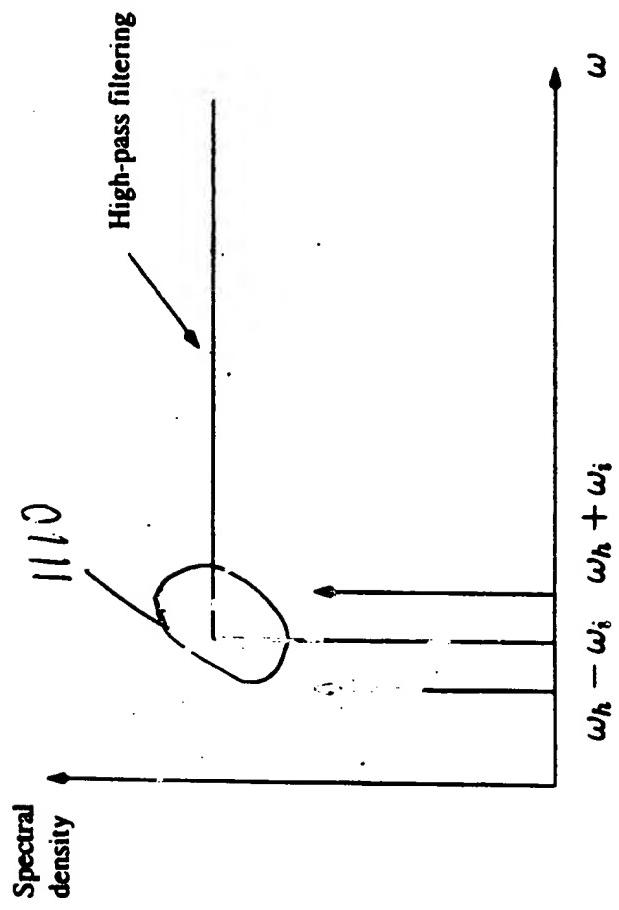


Figure 11

Figure 12

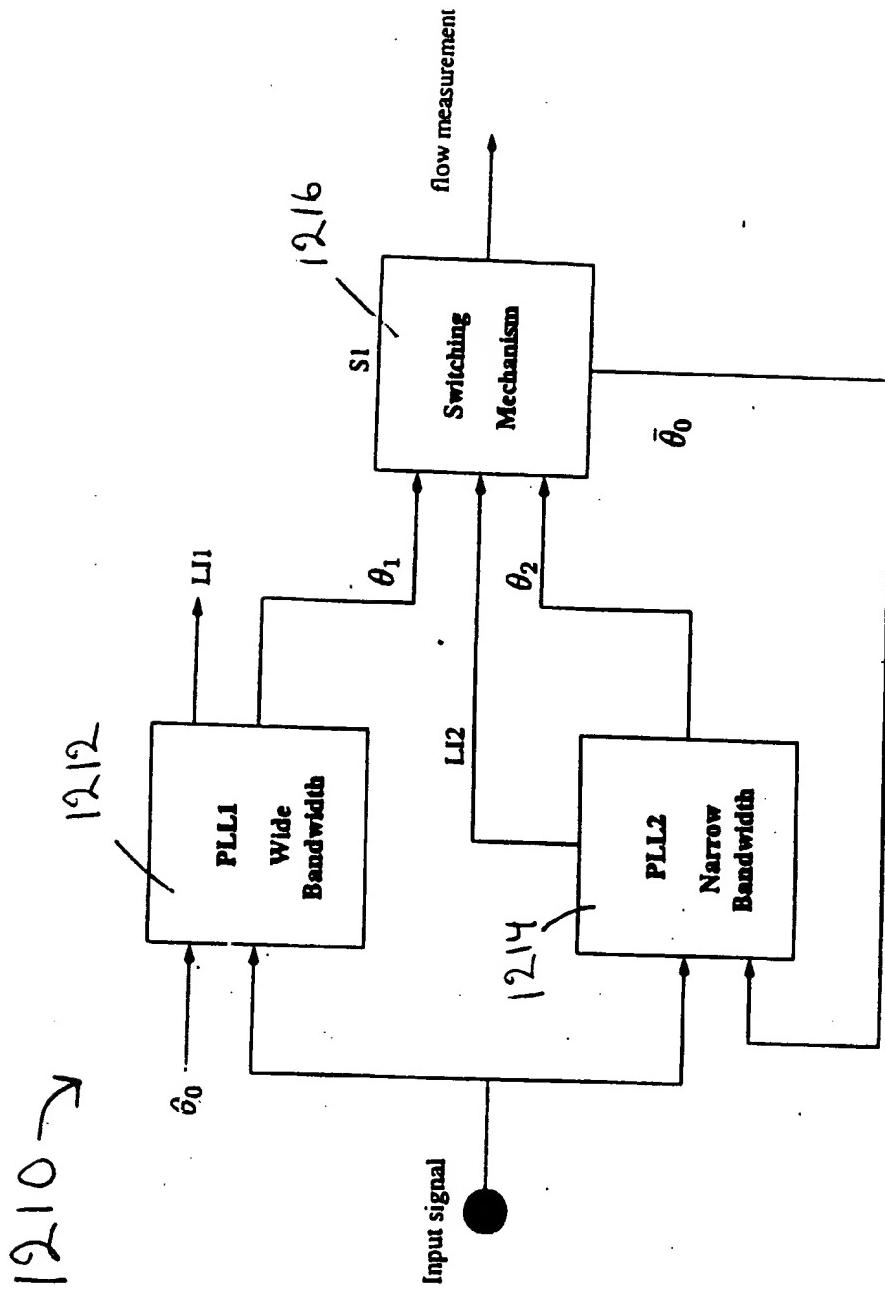
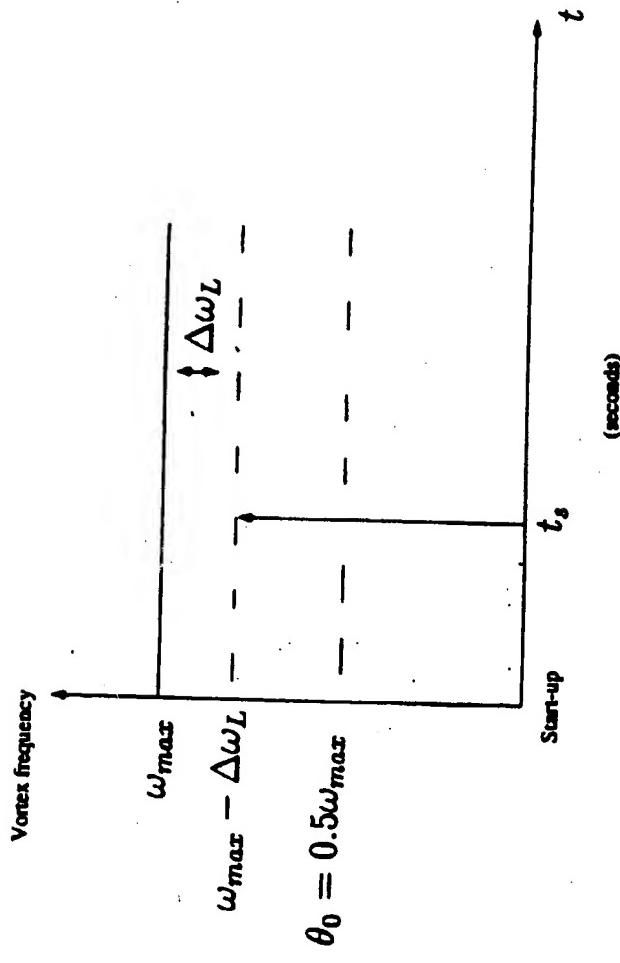


Figure 13



10 12 14 16 18 20 22 24 26 28 30

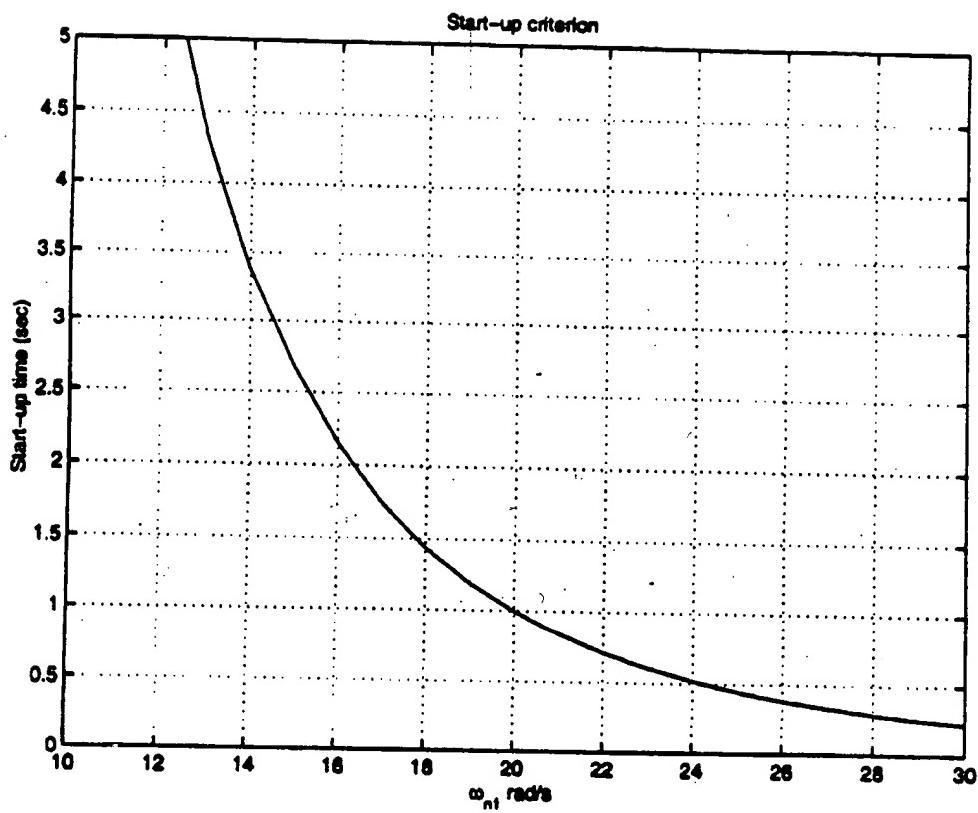


Figure 14.

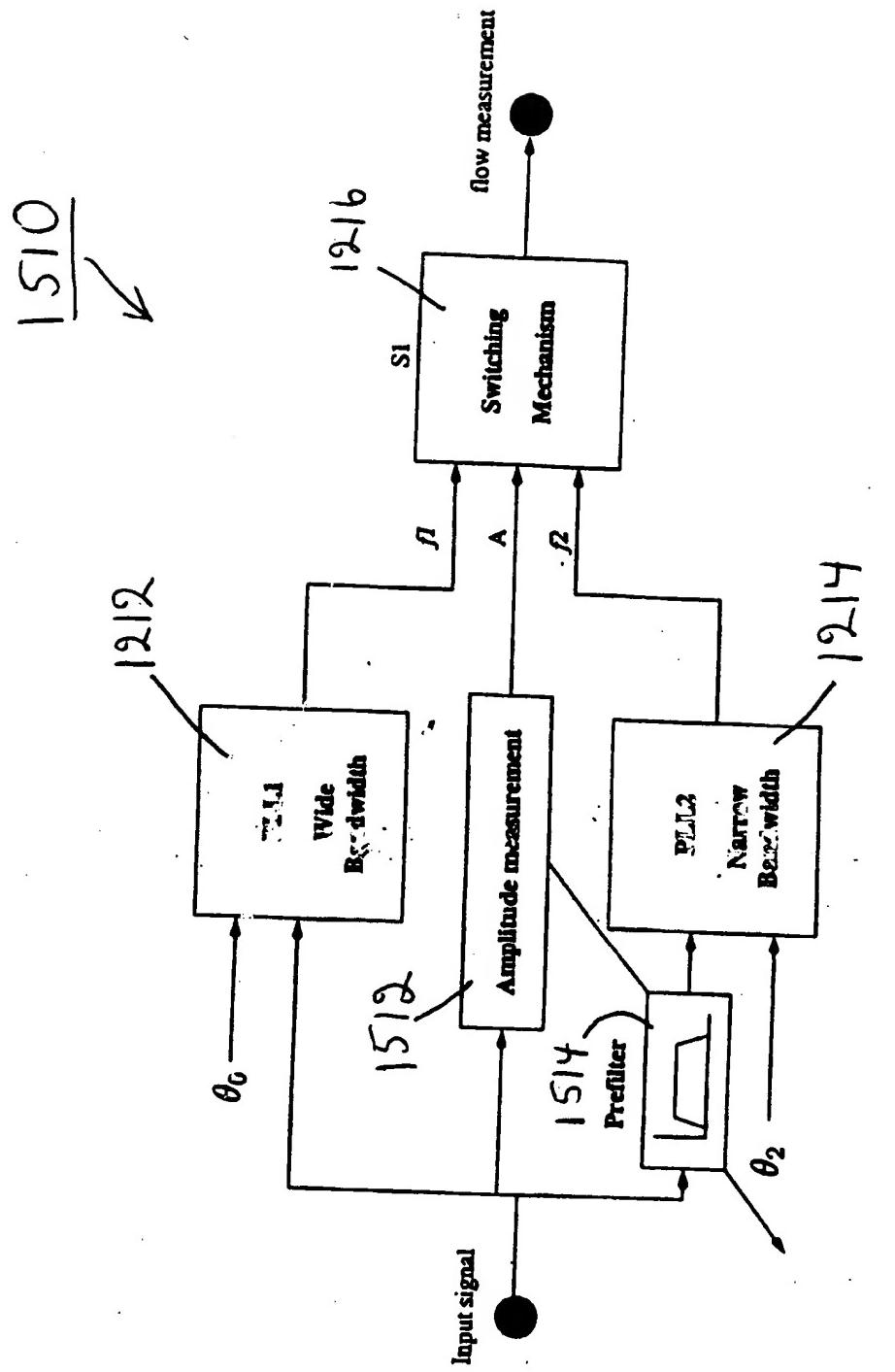


Figure 15

Figure 16

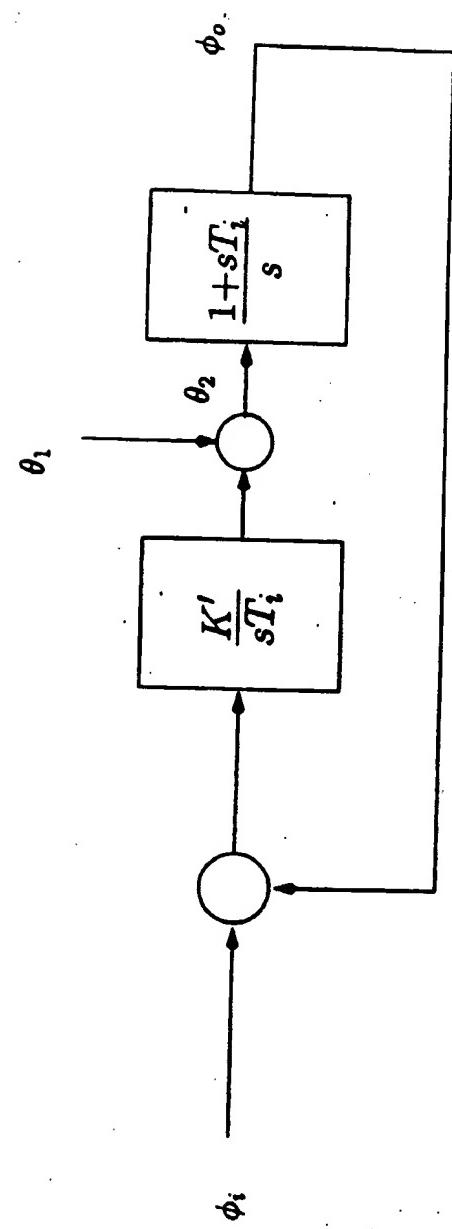


Figure 17

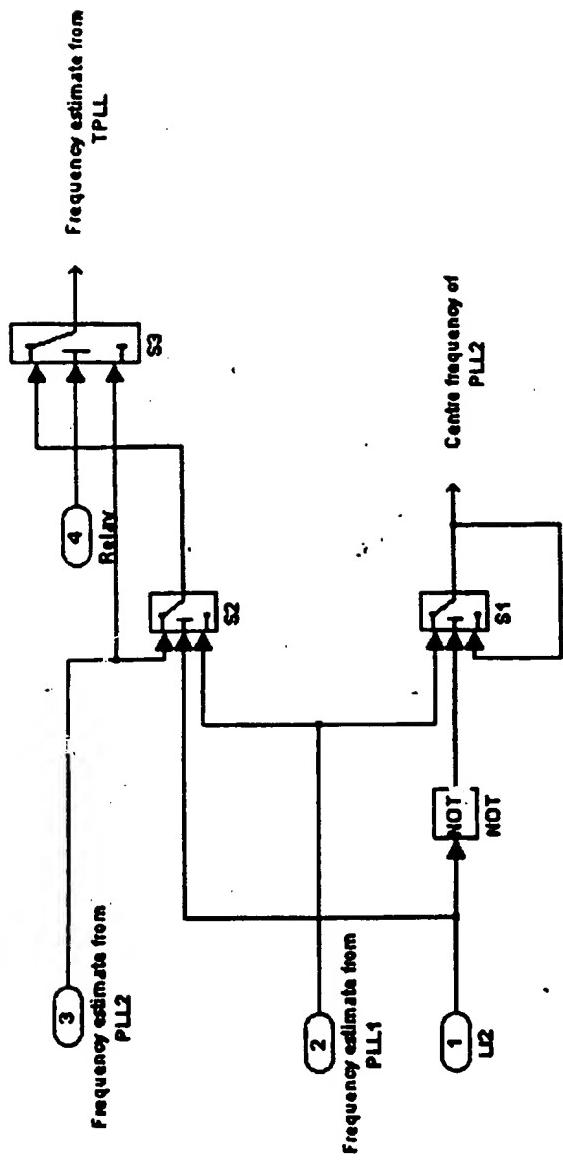
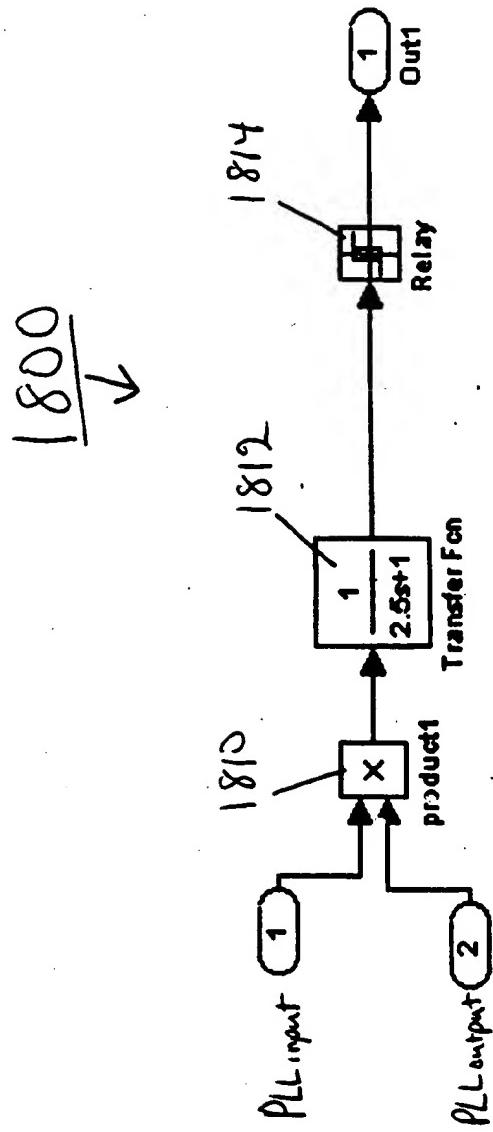


Figure 18



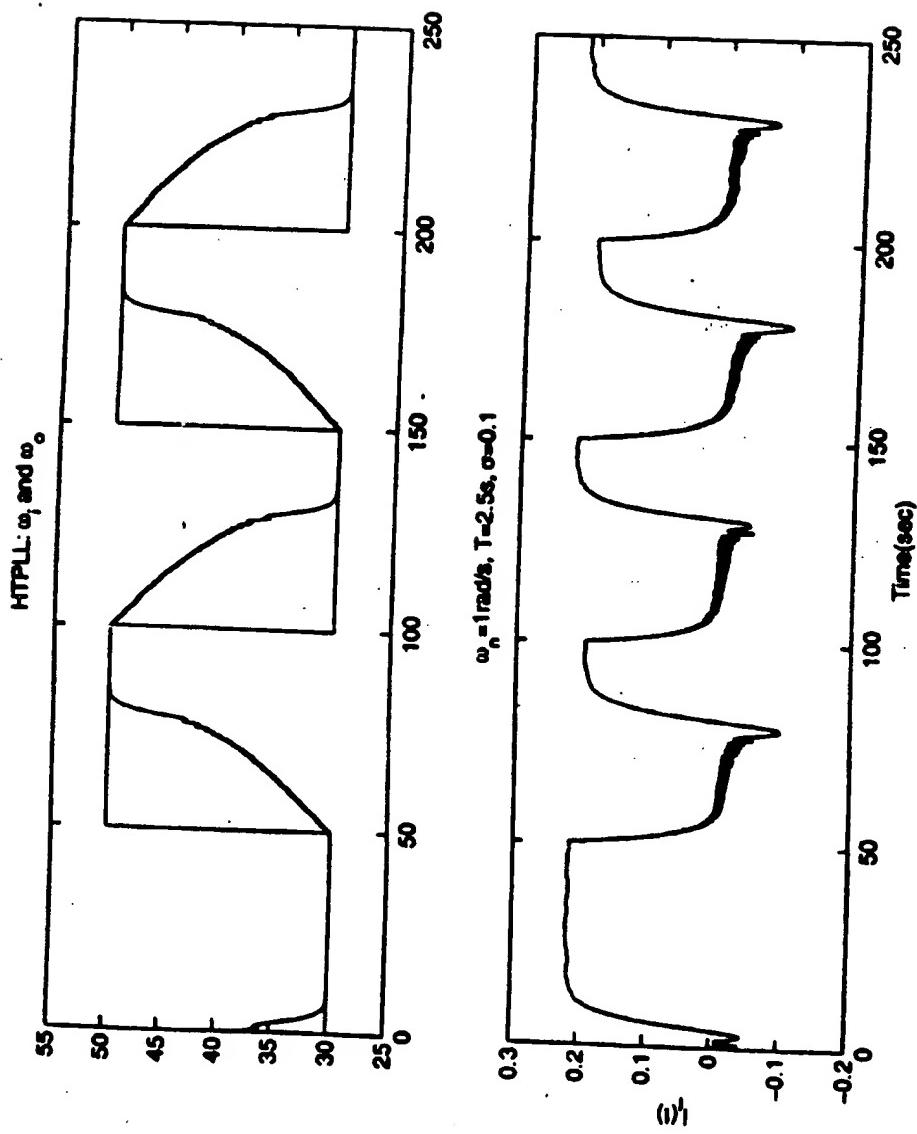
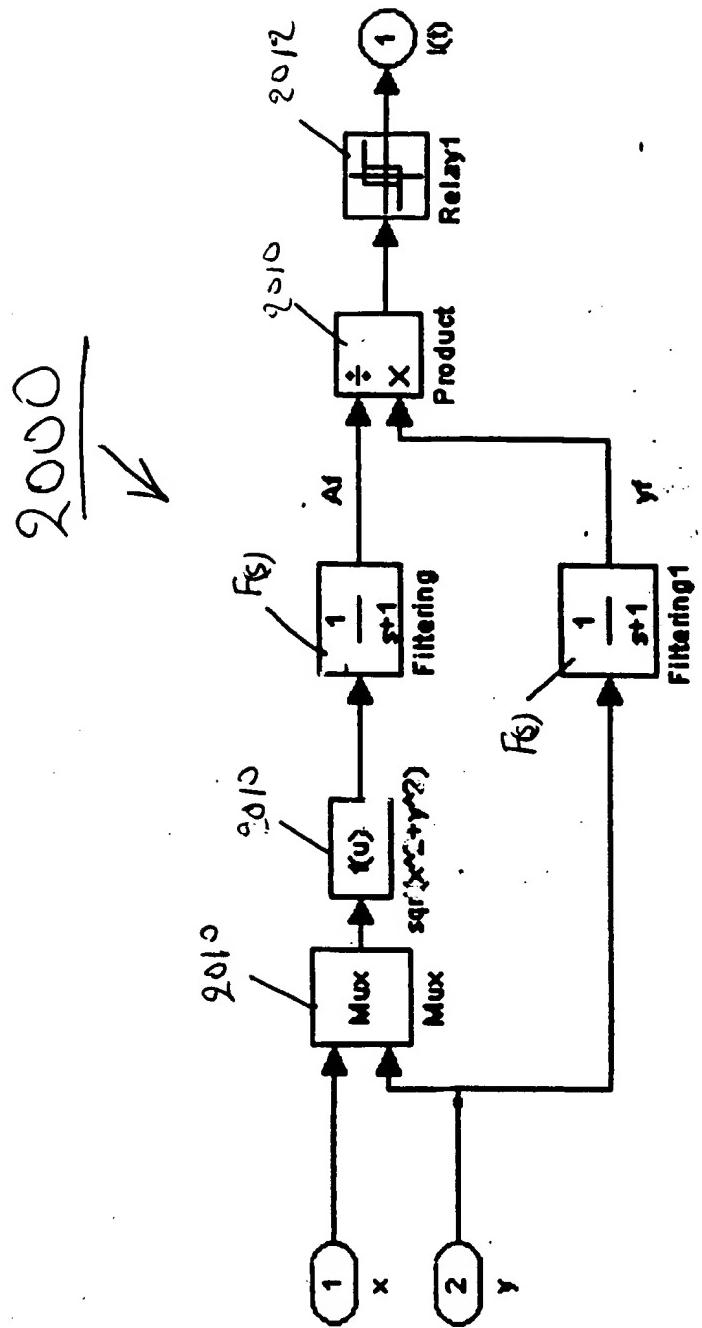


Figure 19

Figure 20



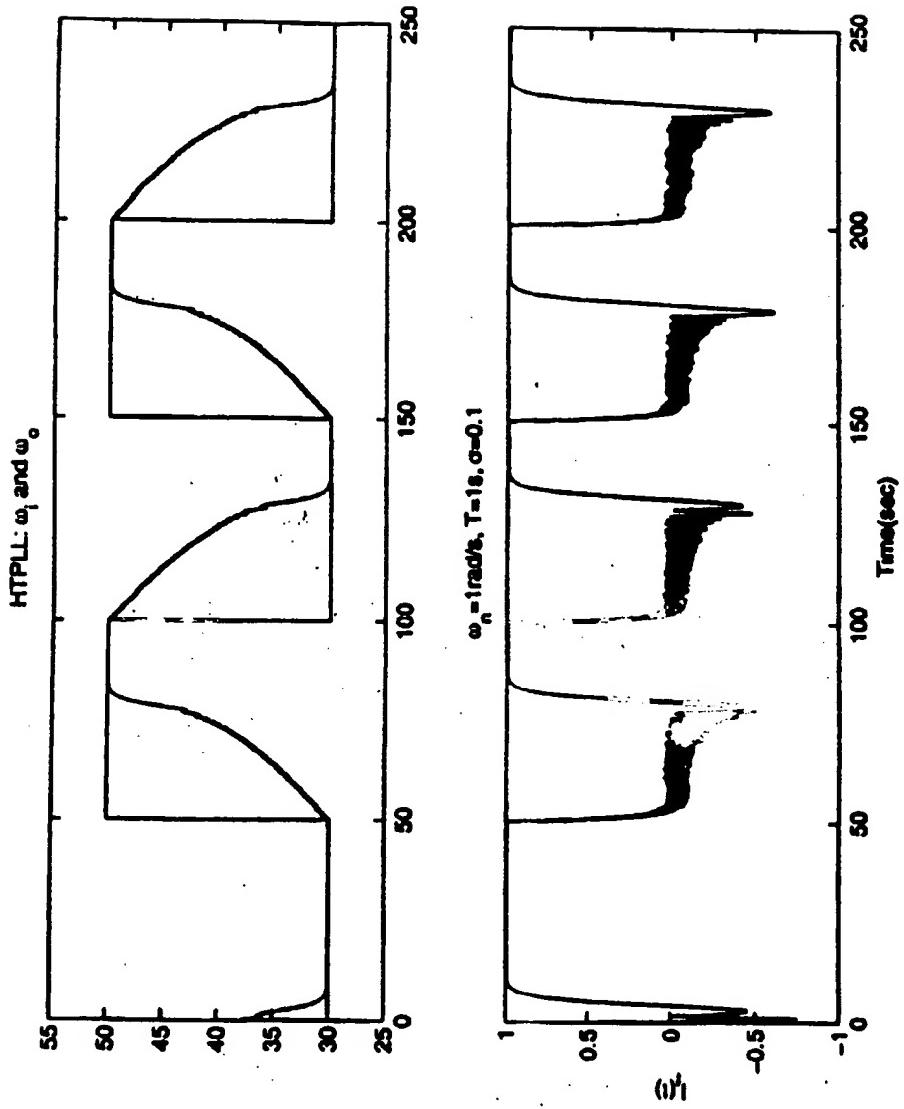


Figure 21

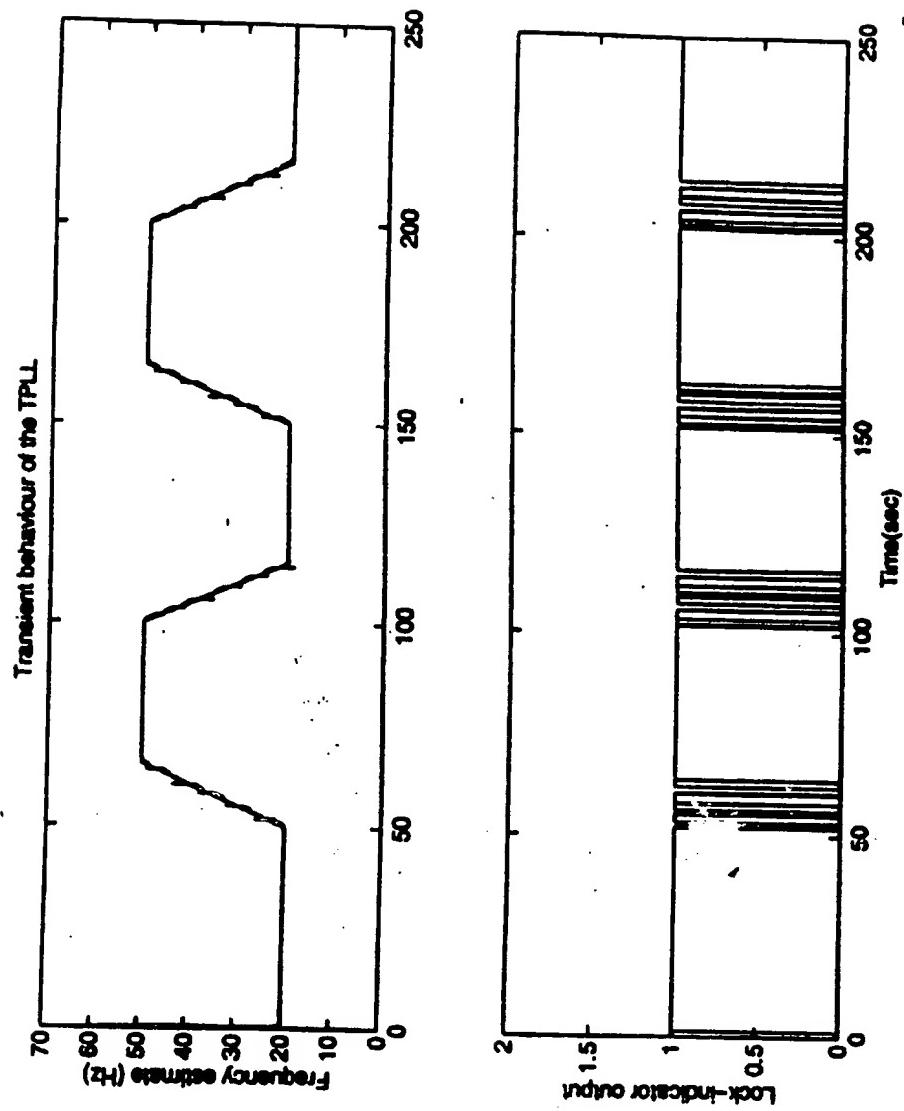


Figure 2.2

2300

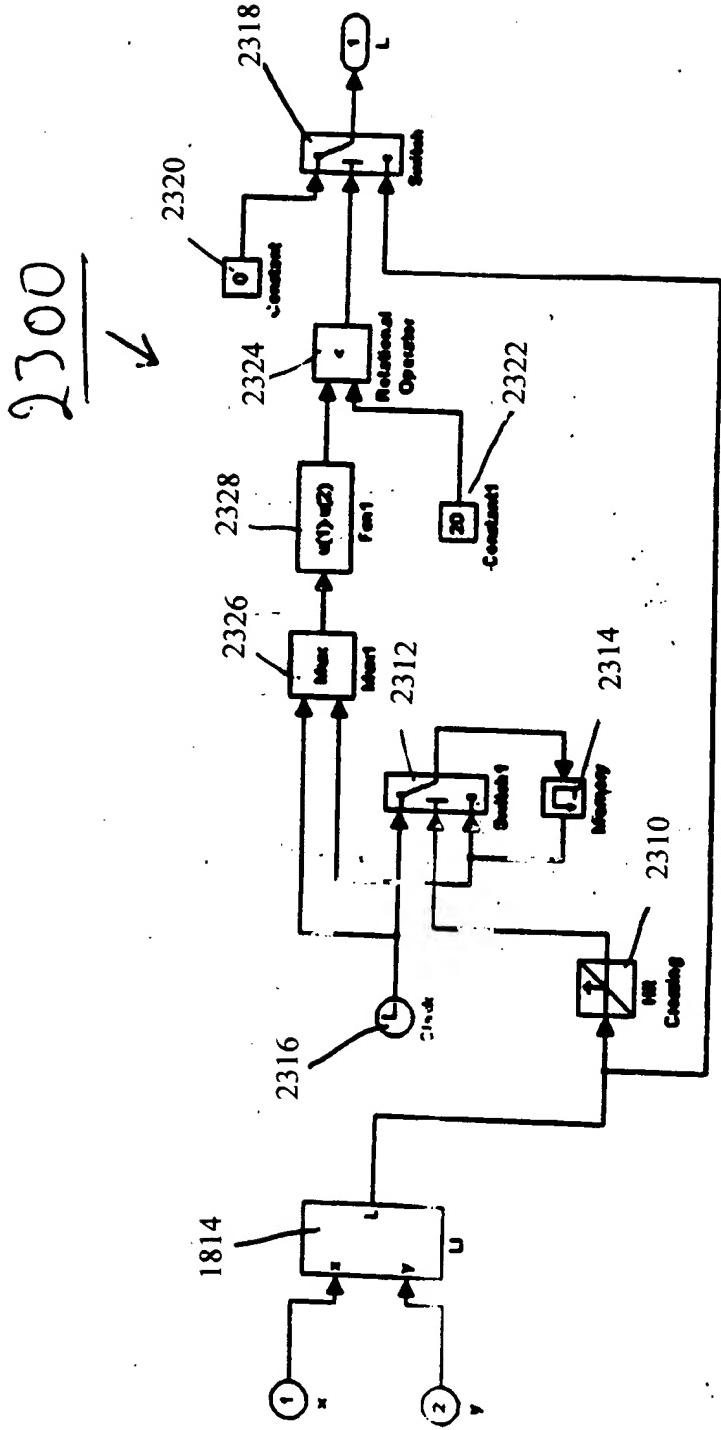


Figure 23

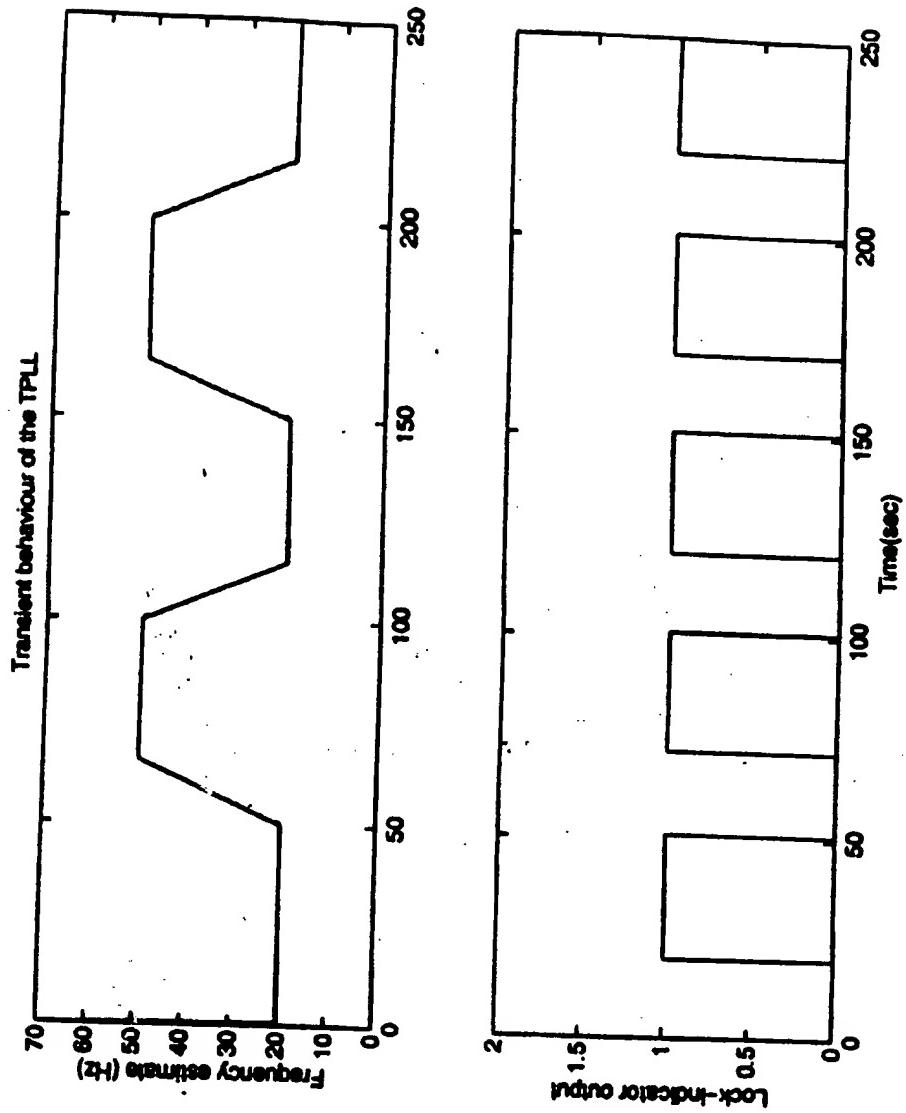
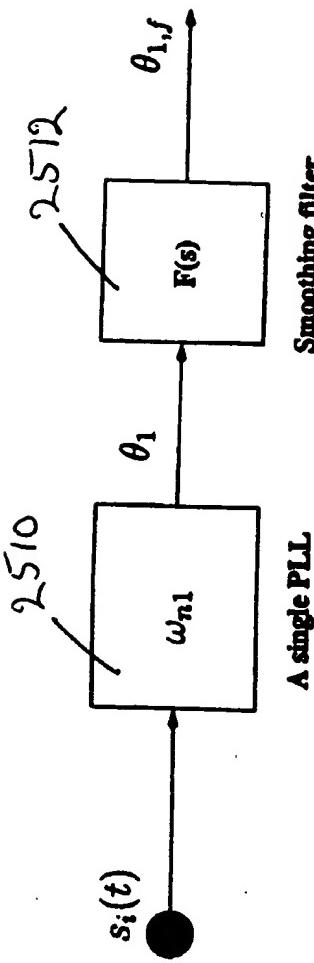


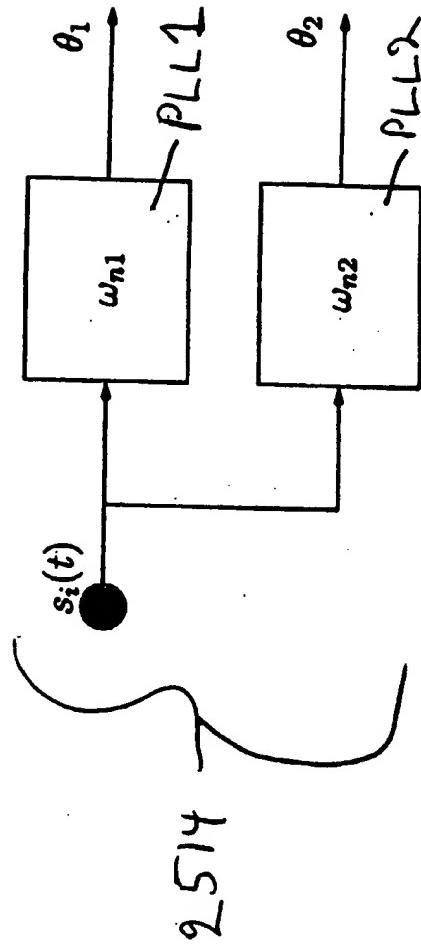
Figure 24

2510 2512



A single PLL

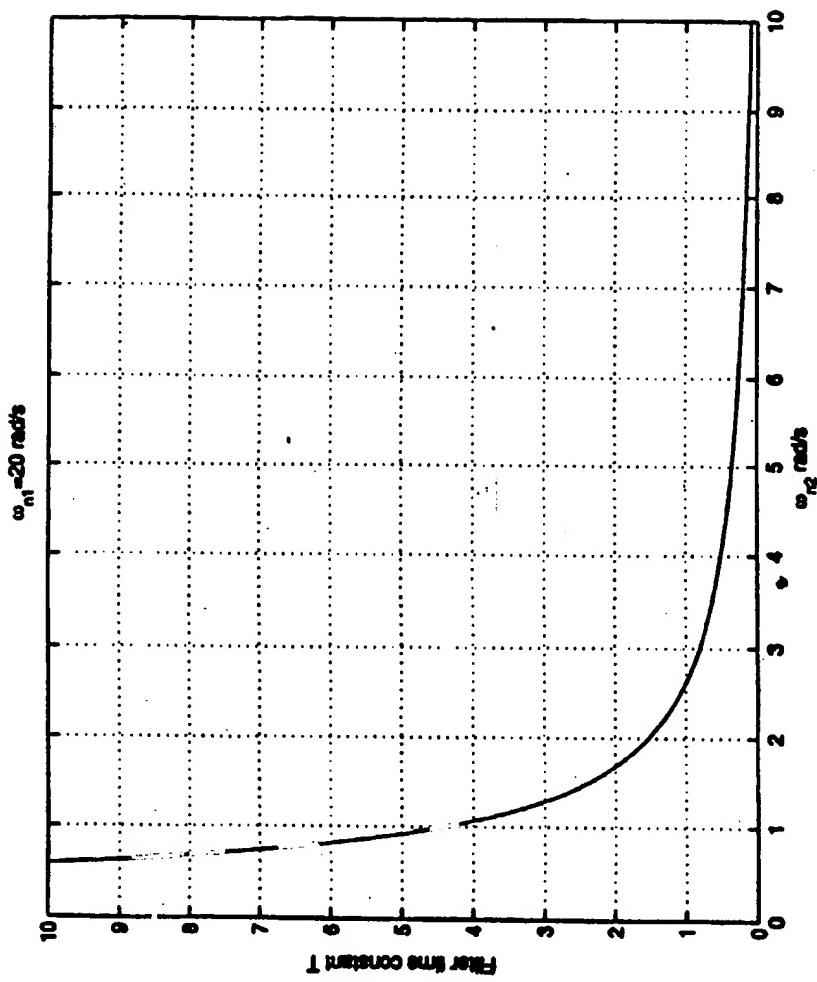
Smoothing filter



Dual PLL Processor

Figure 25

Figure 26



2700



2710

Choose bandwidth of PLL1 based
on start-up performance

2712

Choose bandwidth of PLL2 based
on noise-rejection performance

2714

Design appropriate lock indicator

2716

Choose prefilter bandwidth

2718

Design appropriate relay to
control prefilter

Figure 27

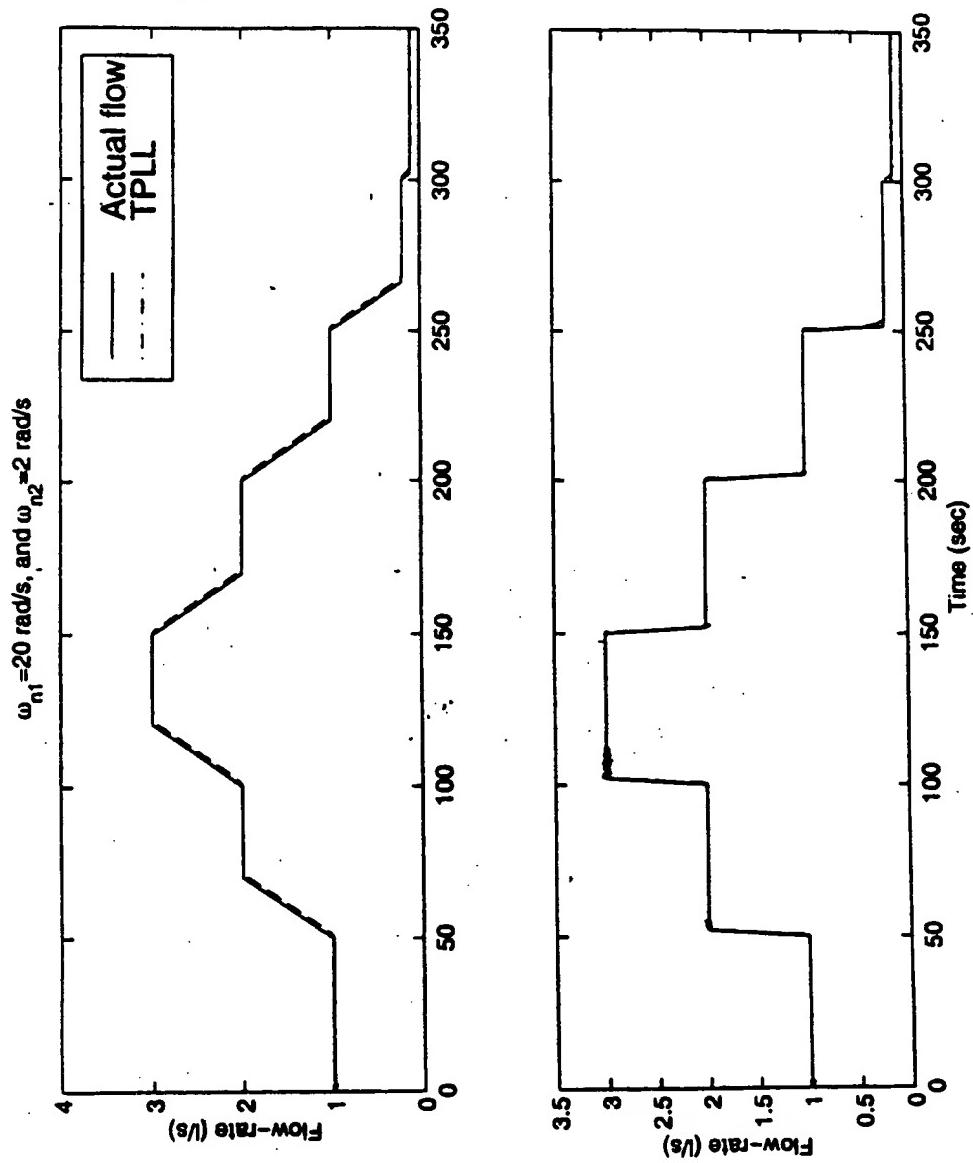


Figure 28

F00080 = 0021F2600

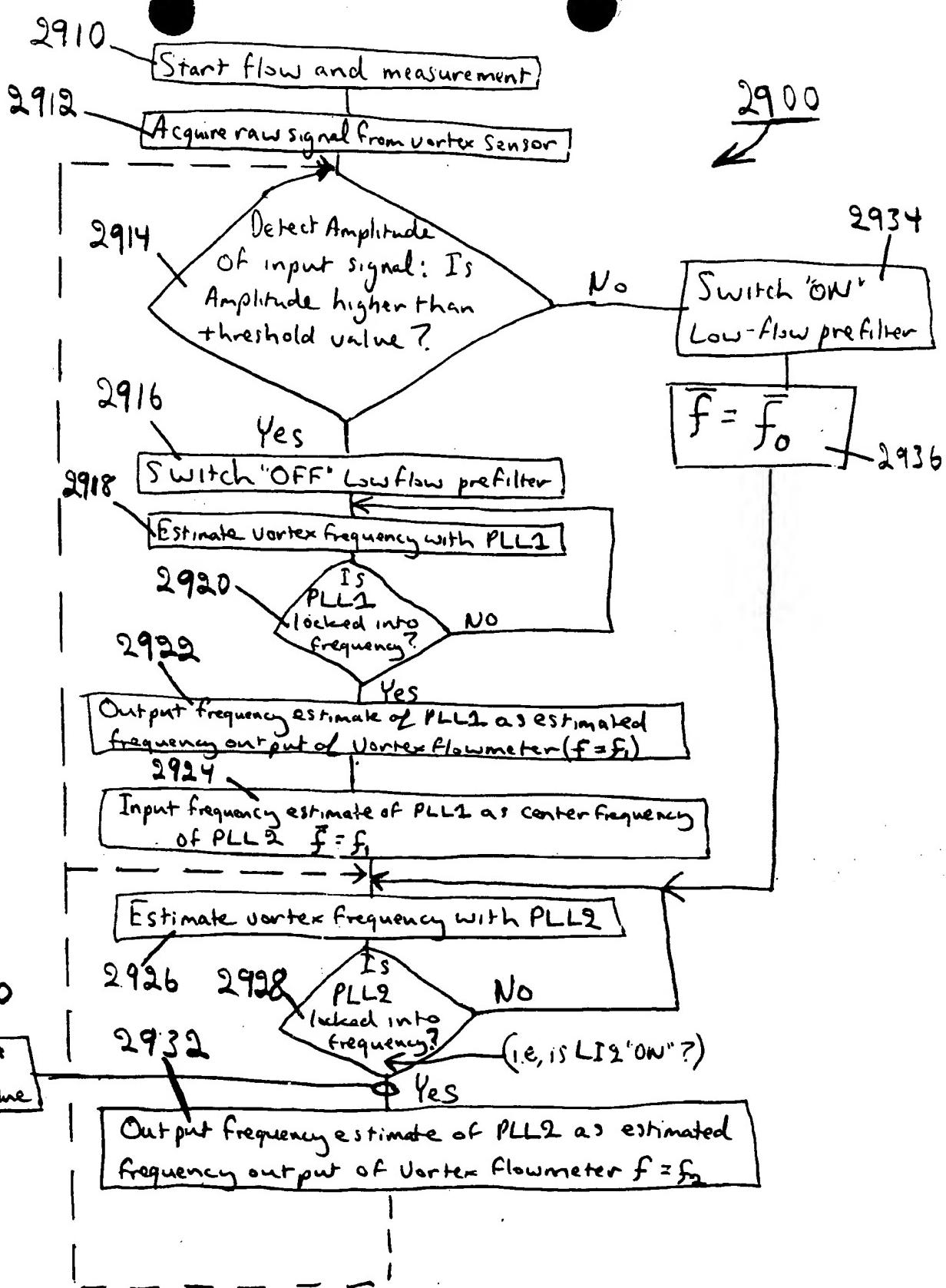


Figure 29

Figure 30

